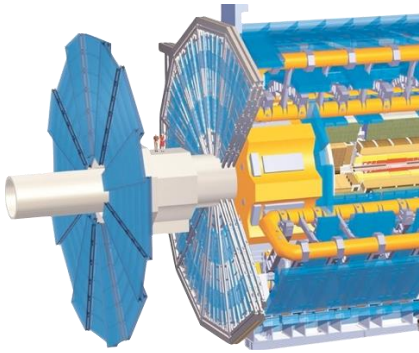
TEXAS
The University of Texas at Austin

ATLAS EXPERIMENT



UT-Austin ADC Design ATLAS LAr Calorimeter at HL-LHC

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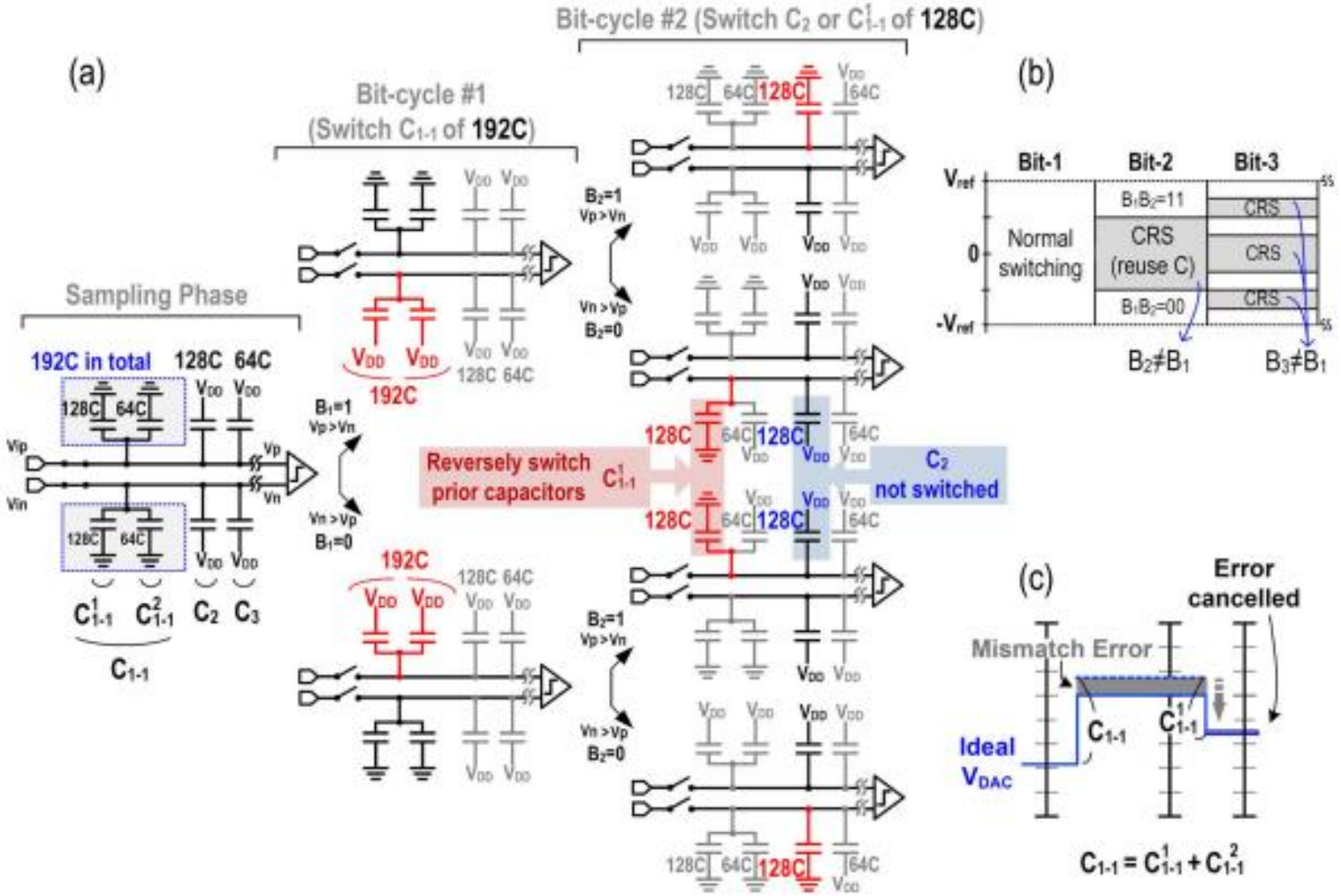
Outline

- Capacitor Linearity Enhancement
- Implementation Progress
- Future work

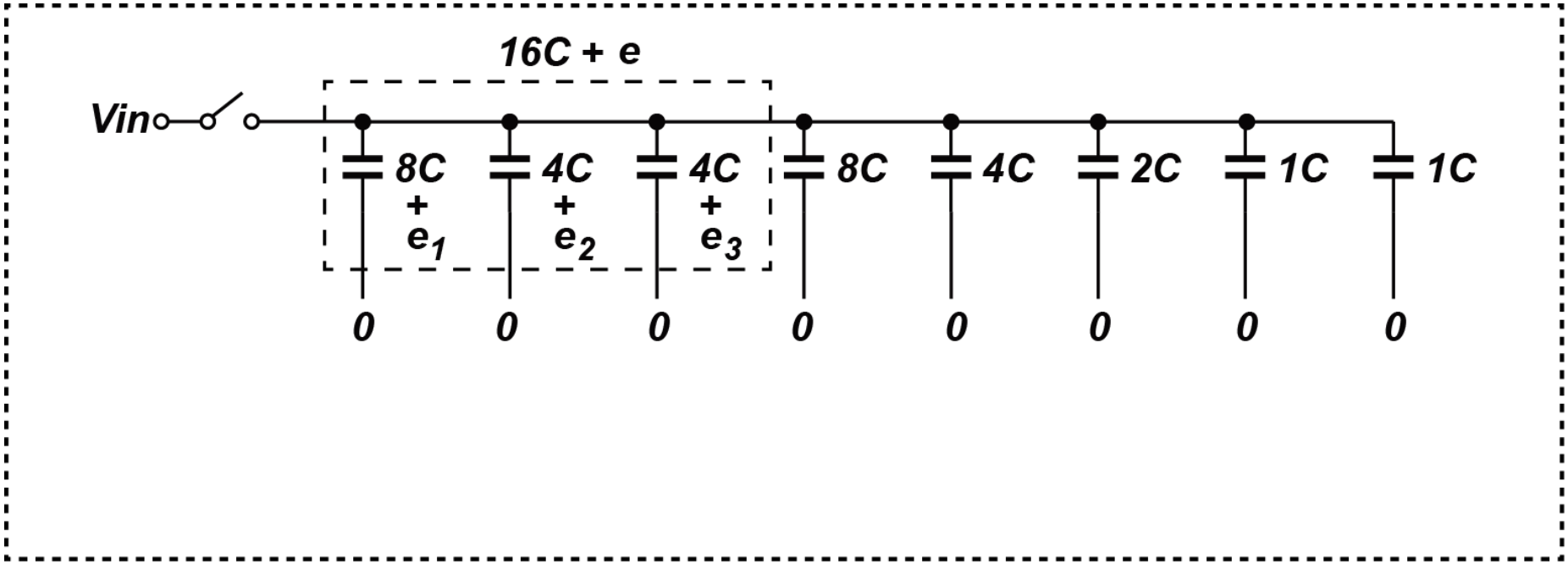
Capacitor Matching Enhancement

- Reversed Switching, RS, [1] JSSCC'15



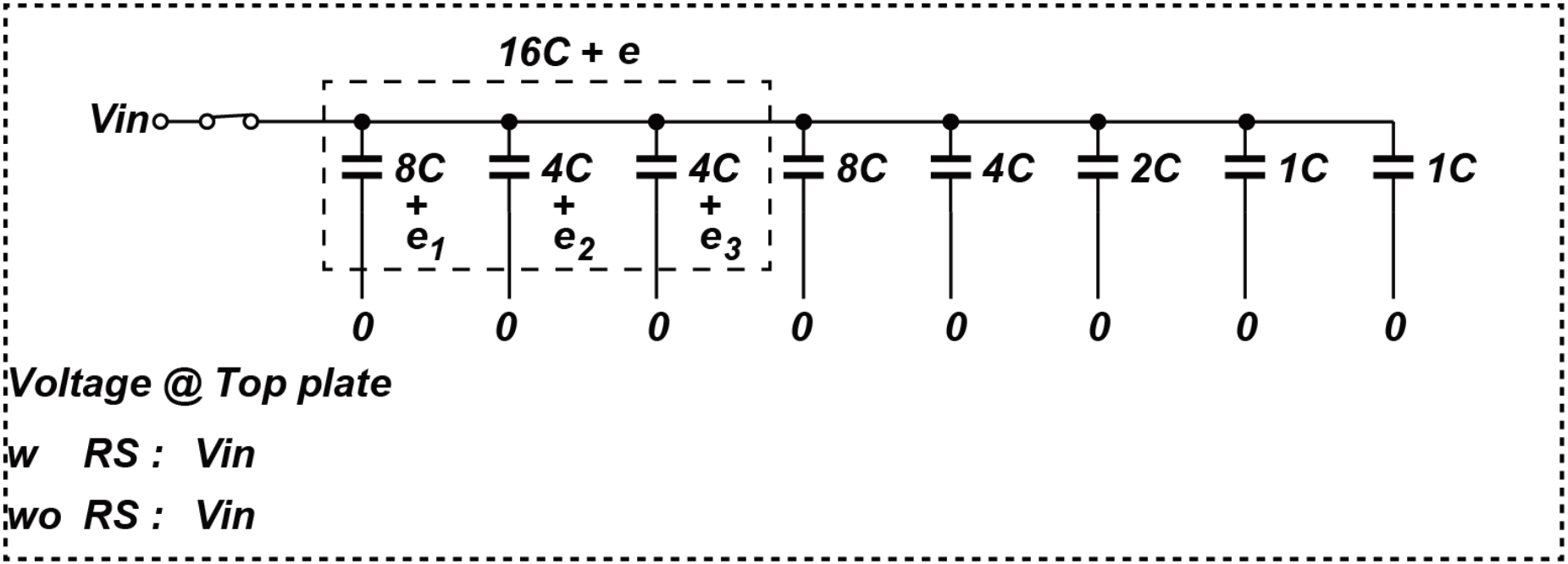
Capacitor Matching Enhancement

- Digital Sequence : 100



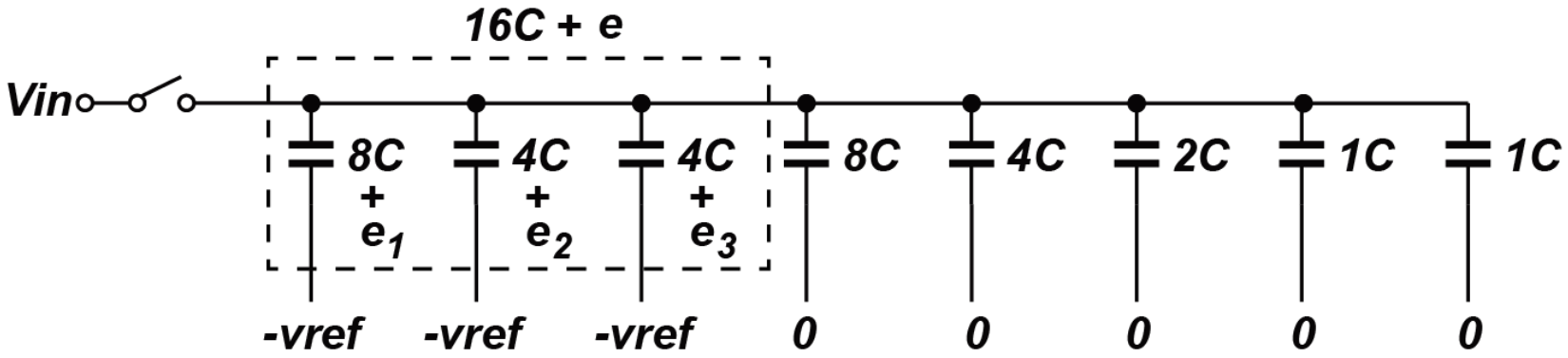
Capacitor Matching Enhancement

- Digital Sequence : 100



Capacitor Matching Enhancement

- Digital Sequence : 100



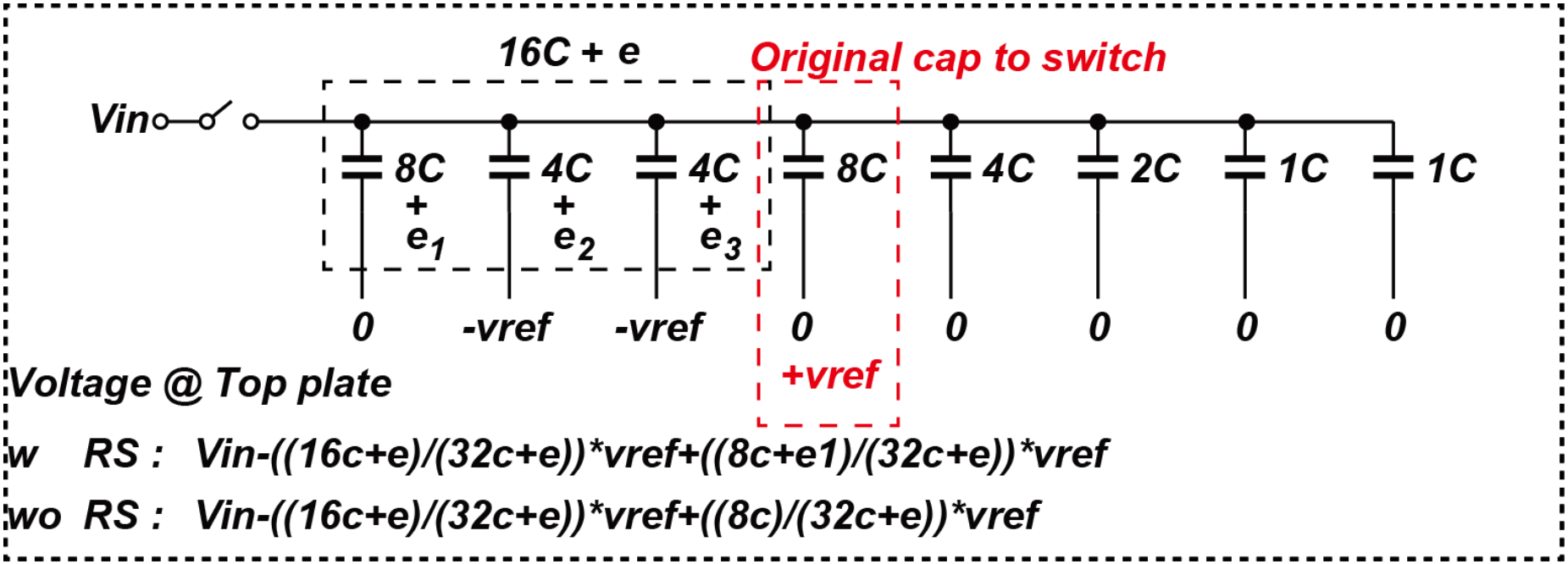
Voltage @ Top plate

*w RS : Vin-((16c+e)/(32c+e))*vref*

*wo RS : Vin-((16c+e)/(32c+e))*vref*

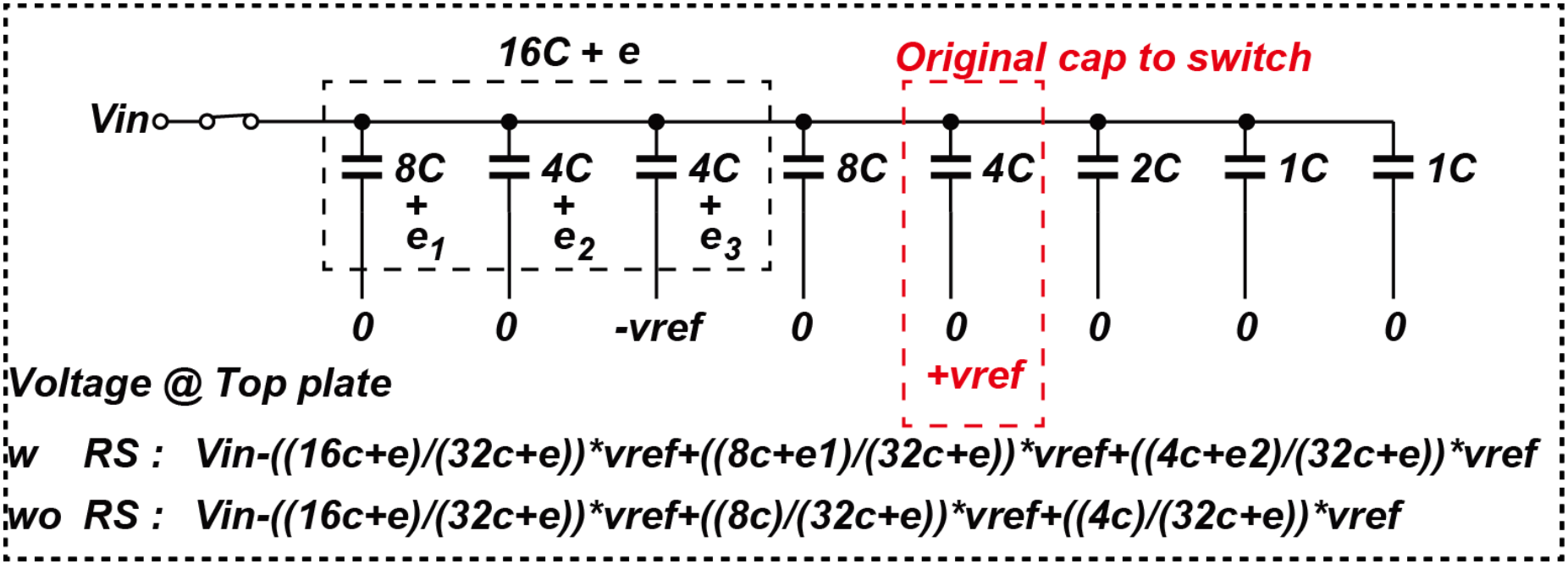
Capacitor Matching Enhancement

- Digital Sequence : 100



Capacitor Matching Enhancement

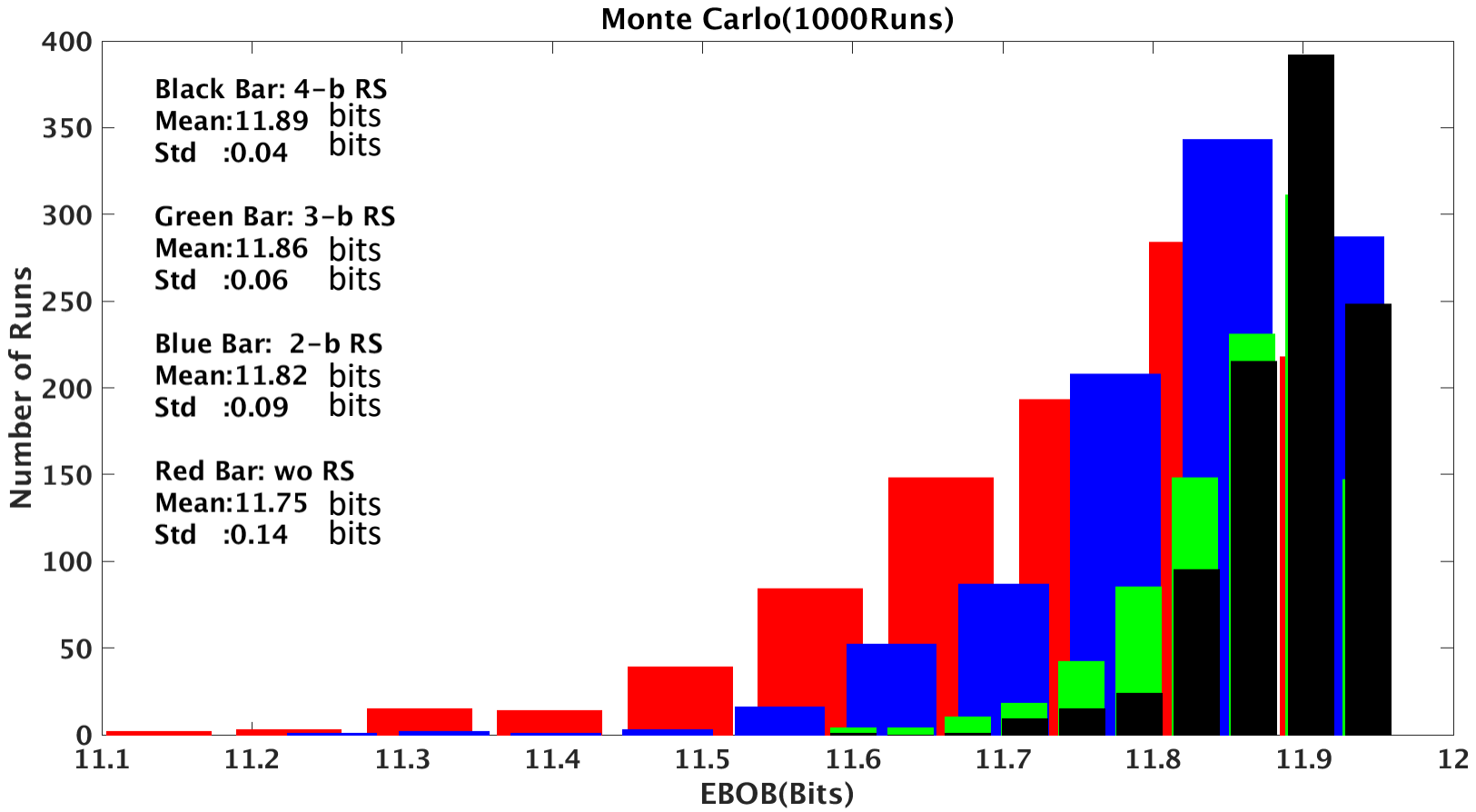
- Digital Sequence : 100



- Remember that e equals to e1+e2+e3

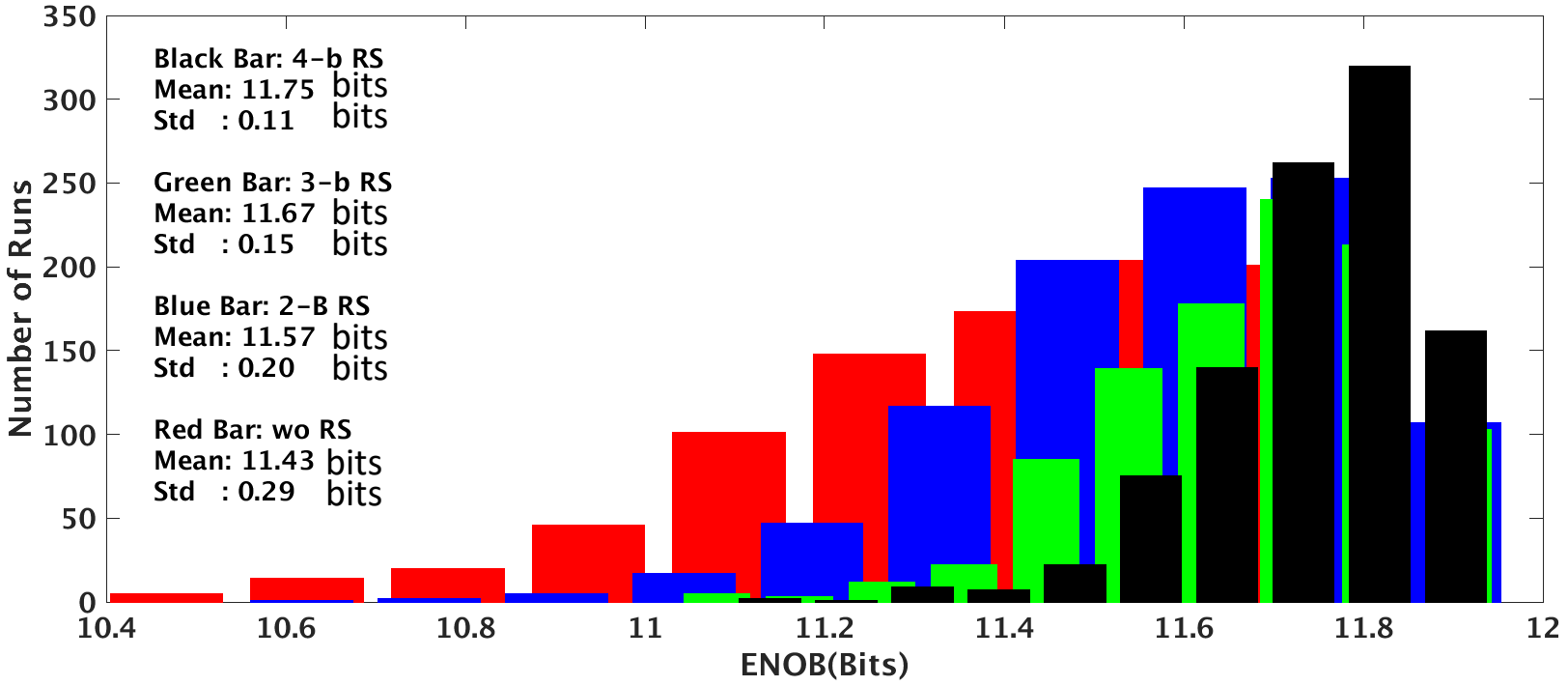
Capacitor Matching Enhancement

- Unit capacitor of 200fF in 1st stage.



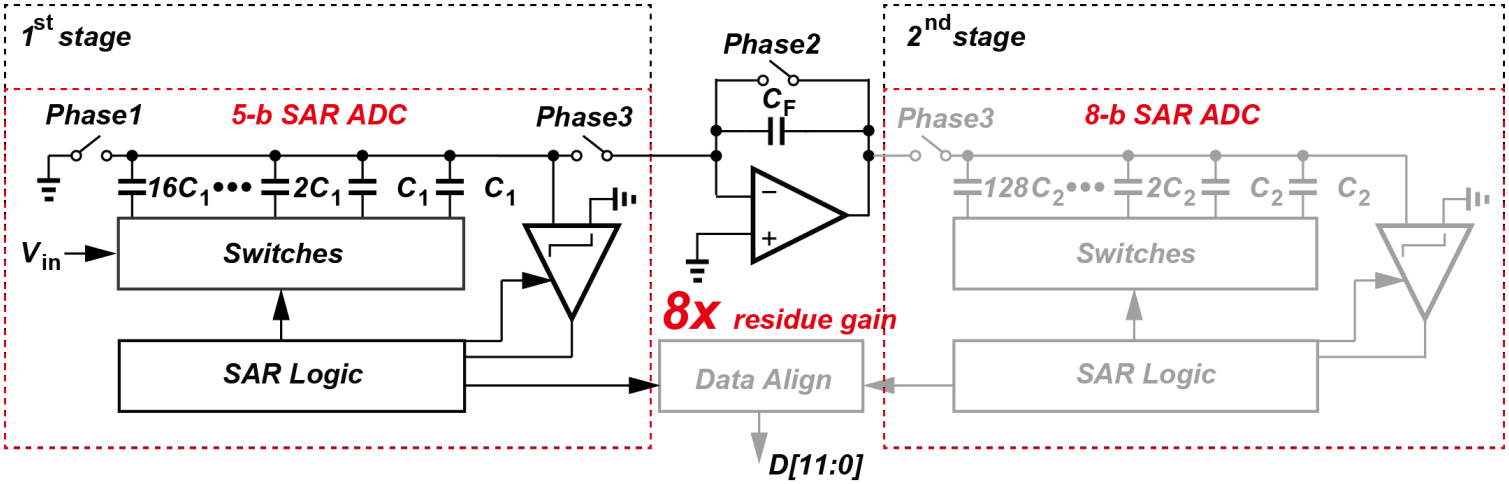
Capacitor Matching Enhancement

- Unit capacitor of 20fF in 1st stage.



Implementation Progress

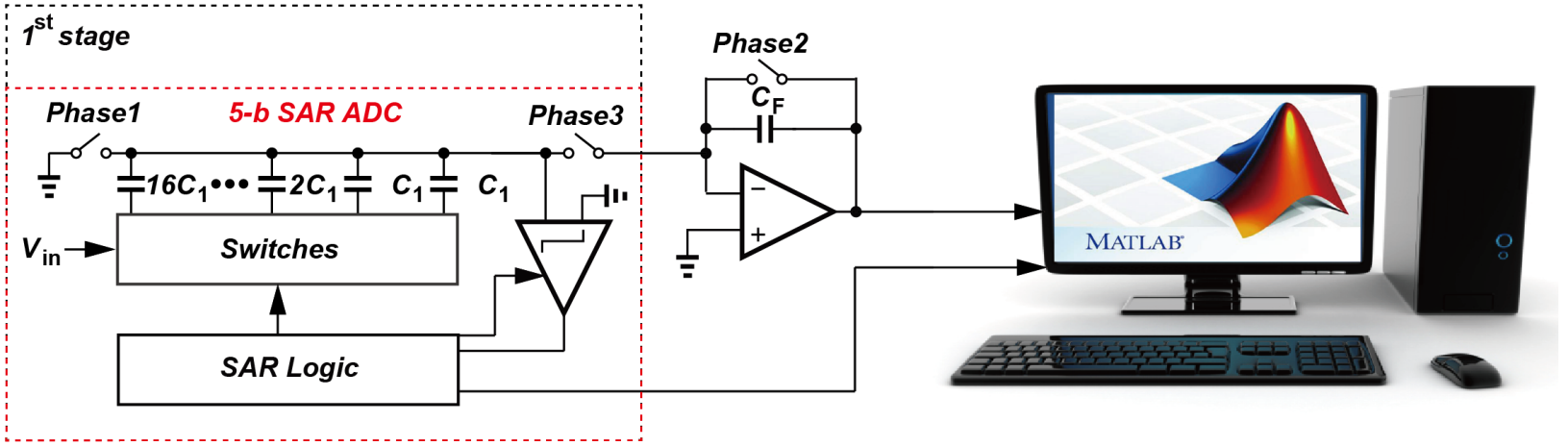
- First stage has been built(without RS).

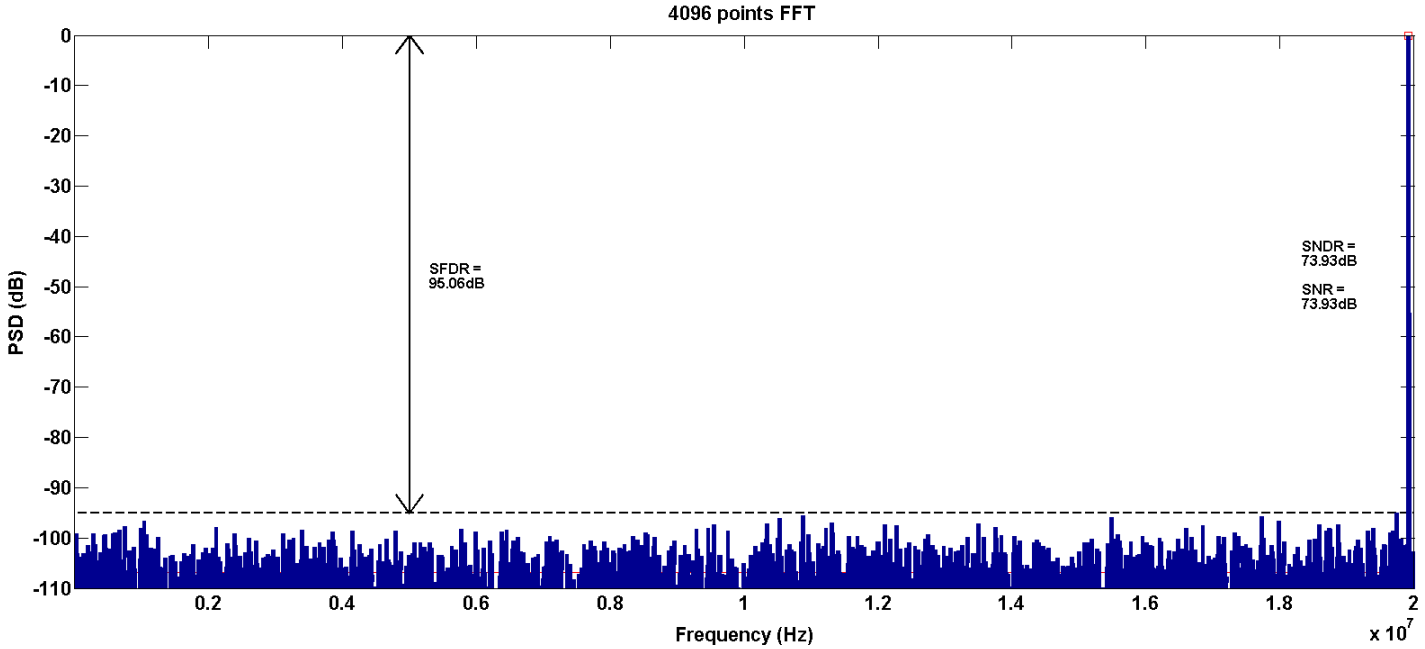


	Power Consumption
OPAMP	1.8mW
1st Comparator	60uW
1st SAR Logic	20uW
Bootstrap Switch	6uW

Implementation Progress

- Feed the residue of amplifier and digital code into Matlab.





Future Work

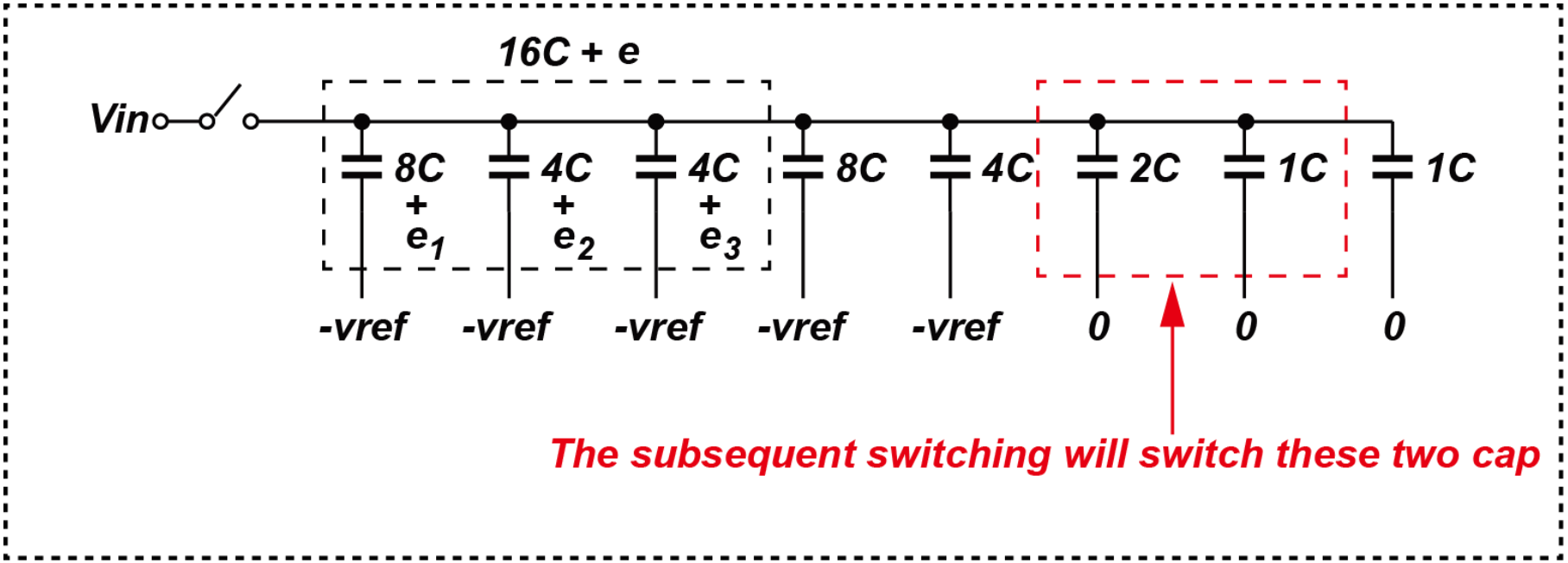
- Implement the RS technique into the first stage.
- Doing more simulation on first stage before next meeting, such as corner simulation and noise simulation.

Reference

1. J.-H. Tsai et al., “A 0.003 mm2 10 b 240 MS/s 0.7 mW SAR ADC in 28 nm CMOS with digital error correction and correlated-reversed switching,” IEEE J. Solid-State Circuits, vol. 50, no. 6, pp. 1382–1398, Jun. 2015.

Backup

If the digitized code is 111, the following switching will not switch back.



Backup

Performing more bits RS will alleviate this dilemma.

Assuming 111 has been resolved and the following sequence will be 00, 01, 10, 11.

Except for 11111, the other sequence will have at least one switching back.